Remark

Applicants respectfully request reconsideration of this application as amended. Claims 1, 7, 13-16 have been amended. Claim 17 is new. Therefore, claims 1-17 are present for examination.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980

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Insertions are underlined and deletions bracketed.

1. (Amended) A method comprising:

receiving real-time analog data at a personal computer implementing a general purpose operating system;

generating a real-time event at the personal computer indicating a request to process the real time data;

determining whether the real-time event has a higher priority than a first event being processed at the personal computer; and

[if so,] processing the real-time event if the real-time event has a higher priority than the first event.

7. (Amended) A computer system comprising:

a chipset;

a bus coupled to the chipset; and

a central processing unit (CPU), [wherein the CPU] coupled to the bus, that operates according to a general purpose operating system, [adaptable to execute real-time instructions] and processes real-time data received at the computer system.

13. (Amended) A central processing unit (CPU) comprising:

a timer to generate timing signals at predetermined time intervals;[and]

an event mechanism coupled to the timer to generate real time events in response to receiving the timing signals and real-time data[, wherein the CPU operates according to a general purpose operating system adaptable to execute real-time instructions.]; and

an event handler coupled to the event mechanism to process the real-time events received from the event mechanism,

the CPU operating according to a general purpose operating system.

14. (Amended) The computer system of claim 13 wherein the CPU further comprises a register coupled to the event mechanism to store real-time data [an event handler coupled to the event mechanism to process real-time events].

15. (Amended) The computer system of claim 14 wherein the [CPU further comprises a register coupled to the event mechanism to store real-time data] event handler verifies whether there is data stored in register upon detecting a real-time event and determines the priority of the real-time event relative to other interrupts received.

16. (Amended) The computer system of claim [15] 14 wherein the CPU further comprises an analog to digital converter coupled to the register.

17. (New)